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Question Paper Code : 40516

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2025.

Sixth/Seventh Semester

Electronics and Communication Engineering

EC 8095 — VLSI DESIGN

(Common to Electrical and Electronics Engineering/Electronics and Instrumentation Engineering/Electronics and Telecommunication Engineering/Instrumentation and Control Engineering/Robotics and Automation)

(Regulations 2017)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Name the types of layout design rules.
2. What is the logical effort of a MOS transistor?
3. Design a 2:1 multiplexer using transmission gates.
4. Differentiate CPL and DPL.
5. Draw the astable multivibrator circuit using MOS transistors.
6. What is the sense amplifier based register?
7. Name the data path circuits used in arithmetic building blocks.
8. What is the significance of memory peripheral circuitry?
9. What are the basic building blocks of FPGA architecture?
10. What is testing? What are the types of testing suitable for VLSI design?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Illustrate the long-channel IV characteristics of MOS transistor. (7)
(ii) Obtain the drain current for linear region of MOS transistor. (6)

Or

- (b) Elucidate the DC transfer characteristics of MOS transistor. (13)

12. (a) (i) Discuss the general structure of cascade voltage switch logic. Design the XOR and XNOR using cascade voltage switch logic. (7)
(ii) Draw the structure of dual rail domino logic. Realize the AND and NAND gates using dual rail domino logic. (6)

Or

- (b) (i) Explain the static and dynamic power of MOS circuits. Obtain the total power. (7)
(ii) Show how low power is achieved in MOS based design. (6)
13. (a) (i) Differentiate latches and flipflops. Explain the static latches and flipflops suitable for sequential circuit design. (7)
(ii) What is pipelining? Apply pipelining for the function $F = \log|a_n - b_n|$, where $n = 1, 2, 3$. Find the total time to obtain all the outputs. (6)

Or

- (b) (i) Describe the monostable multivibrator circuit using MOS transistor. (6)
(ii) What are the timing classifications of digital system? Design a synchronous sequential circuits based on the timing. (7)
14. (a) (i) Draw the architecture of 4-bit carry look ahead adder and explain the operation. (7)
(ii) Design a 4-bit ALU with control logic. (6)

Or

- (b) (i) Explain the memory architecture with necessary blocks. (7)
(ii) Illustrate the core memory array architecture. (6)
15. (a) (i) Elucidate the FPGA inter connect routing procedures for the implementation of logic circuits. (7)
(ii) Explain common testing technique for Ad Hoc testing. (6)

Or

- (b) (i) Examine the boundary scan architecture and illustrate the system level test techniques. (7)
(ii) Elaborate the finite state machine of Test Access Port (TAP) architecture. (6)

PART C — ($1 \times 15 = 15$ marks)

16. (a) Realize the function $F(a,b,c) = \sum m(2, 3, 5, 6, 7)$ using
- (i) Static CMOS circuit (3)
 - (ii) Rationed circuits (4)
 - (iii) Dynamic circuit (4)
 - (iv) Pass transistor logic. (4)

Or

- (b) (i) Design a 4-bit multiplier and draw the architecture. (8)
- (ii) Find the elmore delay parasitic delay and linear delay for the 4-input NAND gate. (7)
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III. THE EFFECT OF THE VARIOUS FACTORS ON THE RATE OF CHANGE

- (1) The rate of change is directly proportional to the initial concentration of the reactants.
- (2) The rate of change is directly proportional to the surface area of the reactants.
- (3) The rate of change is directly proportional to the temperature of the reactants.
- (4) The rate of change is directly proportional to the presence of a catalyst.

It is found that the rate of change is directly proportional to the initial concentration of the reactants, the surface area of the reactants, the temperature of the reactants, and the presence of a catalyst.